Title
Process Development of FlexTrate(TM) Connector for Silicon Interconnect Fabric

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Publication Date
2020

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA

Los Angeles

Process Development of FlexTrate™ Connector for Silicon Interconnect Fabric

A thesis submitted in partial satisfaction

of the requirements for the degree Master of Science

in Materials Science and Engineering

by

Po-Chang Shih

2020

ABSTRACT OF THE THESIS

Process Development of FlexTrate™ Connector

for Silicon Interconnect Fabric

by

Po-Chang Shih

Master of Science in Materials Science and Engineering

University of California, Los Angeles, 2020

Professor Subramanian Srikanteswara Iyer, Chair

Heterogeneous integration is emerging as the mainstay in the performance and scaling enhancement trend. At the Center for Heterogeneous Integration and Performance Scaling (CHIPS), University of California, Los Angeles (UCLA), Silicon Interconnect Fabric (Si-IF) has been established as a heterogeneous wafer-scale integration technology, where bare dies can be mounted on silicon wafer directly with the advantages like fine pitch, small inter-die spacing, lower latency, and higher data bandwidth. As an external communication system for Si-IF, FR4-based periphery connector was investigated earlier but it still has issues such as, CTE mismatch and poor flexibility. To address this problem, FlexTrate™ Connector, a novel flexible device, is proposed. FlexTrate™ is a flexible hybrid packaging platform using fan-out wafer-level packaging method to heterogeneously integrate dies in polydimethylsiloxane (PDMS) substrate.

In this thesis, FlexTrate^{TM} technology is used to fabricate copper wires on PDMS substrate to form a connector that can serve as an external communication system for Si-IF with better mechanical properties, such as better elongation and lower Young's modulus.

The thesis of Po-Chang Shih is approved.

Mark S. Goorsky

Dwight C. Streit

Subramanian Srikanteswara Iyer, Committee Chair

University of California, Los Angeles

2020

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ACKNOWLEDGEMENT

With this opportunity, I would like to thank my advisor, Prof. Subramanian S. Iyer for his guidance and education. Without his support and vision, this work would not be possible. I appreciate Prof. Mark Goorsky and Prof. Dwight Streit for accepting to review this work. Also, I feel grateful to have Mr. Gui-Chun Hung, the vice president at United Microelectronics Corporation (UMC), as my mentor from the industry who advised me in both the career and academic area.

I want to thank Dr. Zhe Wan, Dr. Samatha Benedict, and Prof. Boris Vaisband for their professional advice. In addition, I would like to express my gratitude to Arsalan Alam, Goutham Ezhilarasu, SivaChandra Jangam, Guangqi Ouyang, Yu-Tao Yang, Golam Sabbir, Randall Irwin, Arpan Dasgupta, Arshiya Vohra, and Ko-Ching Hou for their assistance during the research and experiment. I thank all the colleagues, including Kyle Jung who manages administrative affairs and takes good care of us, from UCLA CHIPS.

Lastly, special thanks to my parents, my families, and my girlfriend for their love and support.

CHAPTER 1

Introduction

1.1 Motivation of the Work

At the Center for Heterogeneous Integration and Performance Scaling (CHIPS), University of California, Los Angeles(UCLA), two innovative technologies have been developed: a) Silicon Interconnect Fabric (Si-IF), which is a heterogeneous integration method [1] and will be further discussed; and b) FlexTrate^{TM}, which is an embedded packaging method that enhances the flexibility and bendability of the device [2-4] which will also be introduced in this thesis.

Si-IF has several advantages but there is still a lack of a mature external communication system suitable for Si-IF which can transmit power and signal to the outside world reliably. Although, prototype of FR-4 based periphery connector was developed [5], there are still many issues, such as CTE mismatch and the poor flexibility of this device because of the rigid FR-4 board [5, 11].

Thus, in this article, FlexTrate^{TM} Connector, a new type of external communication device, will be presented with the concept of fan-out technology and the fabrication process of FlexTrate^{TM} to suit for bridging the Si-IF with the outer system. Comparing with FR-4 based periphery connector, the better elasticity and elongation of FlexTrate^{TM} will be used to construct a connector compatible to the Si-IF and other similar structures as well.

1.2 Silicon Interconnect Fabric (Si-IF) Technology

With the slowdown of Moore's Law, heterogeneous integration has been developed as a solution in the semiconductor industry. At CHIPS UCLA, Silicon Interconnect Fabric, a novel

heterogeneous assembling technology, is developed to achieve broader bandwidth, lower latency, and reduced power consumption per bit, as shown in Figure 1.

Si-IF, is a platform where the bare dies can be attached directly with well-defined wiring patterns during back-end-of-line processing. Si-IF can achieve very fine pitch (2 to 10 μm) and a small inter-die spacing (less than 100 μm) which can remove the requirement of the additional functional circuit, such as serializer/deserializer (SerDes), and further, reduce the latency, lower the energy consumption and increase the bandwidth of the signal [1, 6].

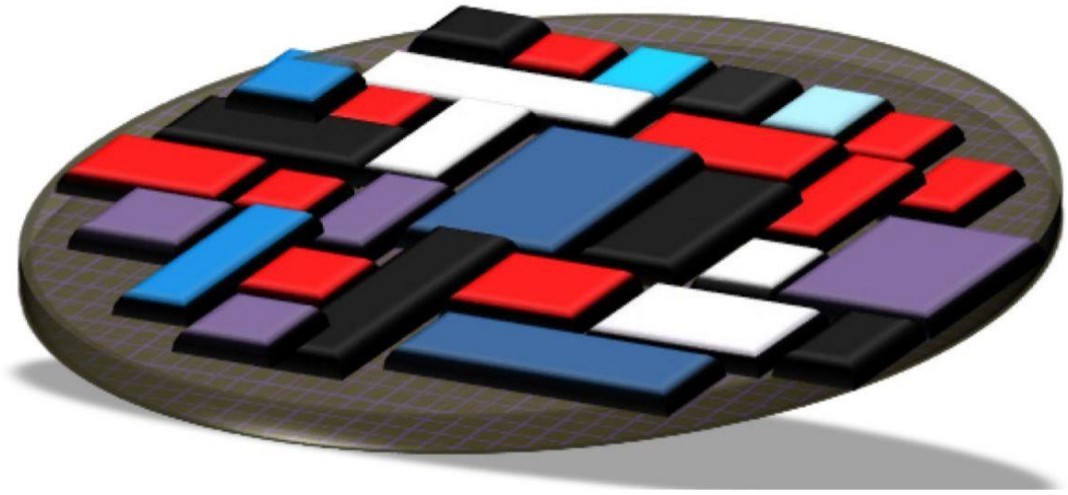


Figure 1. Schematic of Si-IF with mounted dielets [1]

1.3 FlexTrate™ Technology

Commercially, there are two main methods to make the wearable electronic devices flexible. One, called flex-rigid PCB, is an assembly of chips on printed circuit board (PCB); and the other is flexible hybrid electronic (FHE) packaging, in which the thinned bare dies are integrated onto an organic flexible substrate [7]. However, there are some issues with both these methods. For the flex-rigid PCB, the bendability is very limited due to the finite flexibility of PCB.

For the FHE [7], although it has higher flexibility, the process of die thinning will lead to a relatively low yield; adding to this is the low I/O count of FHE, which cannot meet the requirement of high-performance devices [4]. Thus, UCLA CHIPS has developed Flextrate^{TM}, a novel flexible packaging technology, that enables heterogeneous integration by embedding the bare dies into soft flexible materials, such as Polydimethylsiloxane (PDMS), and further interconnecting with fine pitch wiring, as shown in the Figure 2.

PDMS, the soft flexible substrate of FlexTrate^{TM}, improves the bendability of the bare dies which are embedded into the PDMS substrate, with flexibility all the way down to 1 mm bending radius. The flexibility is better than the commercial flexible wearable electronic devices mentioned above [4]. With fine Cu wires (< 40 μm), extra space can be dedicated to I/Os to meet the higher packaging demands [3].

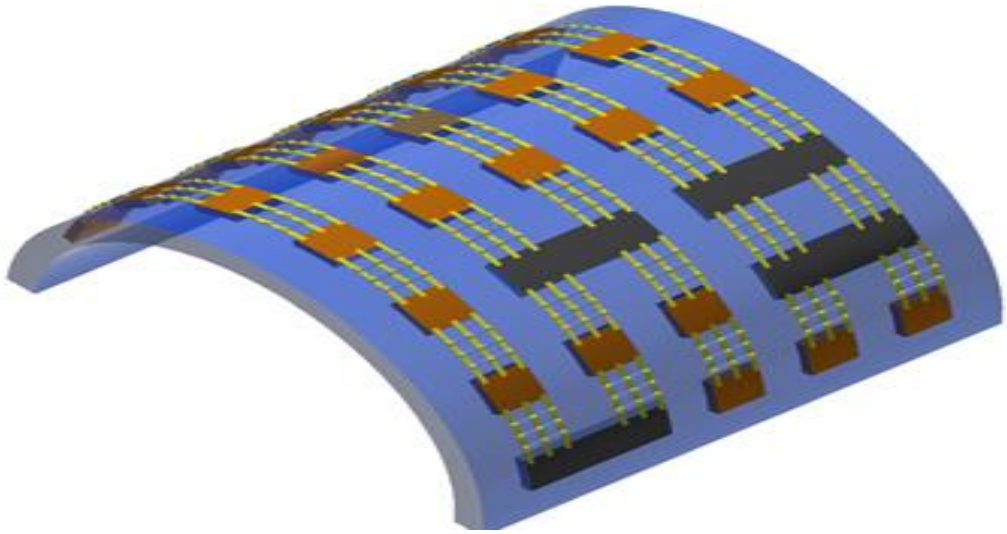


Figure 2. Schematic of FlexTrate^{TM} with multiple dielets connected. [4]

1.4 Electromechanical Connector

A connector is an electromechanical device that connects the ends of two different systems to form a complete circuit so that the power or signal can be transmitted through [8, 9]. A connector can be divided into two parts: conductor, which passes the current, and insulator, which protects the conductor from contamination, short circuit, or other damage. For the conductor, three properties are important: (1) conductivity: the ability to transmit the signal; (2) strength: a mechanical property of the material that represents the response of the solid to stress and strain; (3) plasticity: the ability that shows the plastic deformation of metal [8-10]. For the insulator, the materials should have high resistance and be able to tolerate high temperatures generated from the conductor.

1.5 FlexTrate^{TM} Connector

The aforementioned, FlexTrate^{TM} Connector is a novel electromechanical device that combines the concept of fan-out and FlexTrate^{TM} packaging. By using imaging and electroplating with certain parameters, such as power-level (dose of laser) and current, the copper wiring pattern can be patterned on the substrate of Flextrate^{TM}. Further coating with the passivation layer as the protection and via openings of the contact area for connecting and soldering.

The advantages compared with commercial connector are as follows. Firstly, the pitch of the FlexTrate^{TM} Connector can be minimized to 40 μm, with 20 μm width and 20 μm spacing, which is much smaller than the commercial connector and will lead to a relatively high I/O count. Next, because of the excellent flexibility and elongation of the PDMS substrate, it can overcome many mechanical issues such as cracking caused by thermal shear stress.

Lastly, also the most crucial part, the process of FlexTrate™ Connector can be done at low temperatures ($< 100^{o}C$), which leads to excellent process stability and reliability.

1.6 Objective of the Work

The purpose of this work is using FlexTrate™ as the technology to develop the connector and optimize the process to accommodate the circuit of Si-IF to communicate to the external system. The main contributions of this work are as follows:

1) Developing and optimizing the fabrication process of FlexTrate™ Connector on PDMS substrate.
2) Determining and modifying the rules of the copper wiring pattern.
3) Choosing a viable integration method.

1.7 Organization of the Work

In this thesis, the introduction is mentioned above. This is followed by the design rules of the wiring pattern for the FlexTrate™ in Chapter 2. Further, in Chapter 3, the fabrication process is introduced. After which, the integration methodology is researched in Chapter 4. In Chapter 5, the conclusion is summarized along with future work.

CHAPTER 2

Design of the FlexTrate™ Connector

2.1 Overview of the Design Pattern

For a high-performance device, like Si-IF [6], the frequency of operation is very important. The factors, such as the RC time constant and the density of the wires, that determine the frequency of the device sometimes can be modified with the wiring pattern [11]. Thus the design of the wiring pattern for the FlexTrate™ Connector is one of the most important parameter.

Here, in the case of this work, the pattern is designed to fit the 26 by 26 outputs, which is divided into 13 by 13 outputs per quarter area, from the fan-out pattern of the Si-IF, which is already designed and fabricated. Because of the limitations, like the restriction of the area and the fashion of connecting, which will be addressed in Chapter 2.3, the designing of FlexTrate™ Connector in this work will mainly solve these limitations and fit the pattern of the Si-IF and the outer system. And, lastly, the electrical properties of the designed connector can be measured, analyzed, and further, modified.

2.2 FlexTrate™ Connector Designing

The FlexTrate™ Connector plays the role of the bridge to connect the Si-IF system to the external system. In this section, the design of FlexTrate™ Connector is addressed, which includes the contacts of the internal and external system, and the wires to link the two systems. As a result, the design of the FlexTrate™ Connector will be separated into three parts: (1) the internal contact,

which in this case is the fan-out pattern of the Si-IF; (2) the external contact; and (3) the wiring to connect the internal and external system.

As mentioned above, the pattern of this work should fit the Si-IF 26 by 26 outputs pattern, which shown in the Figure 3. The outer quarter patterns are the fan-out of the inner pattern, which are the outputs of the die packaged with the Si-IF method. The dimension of the outer fan-out pad is 500 μm width and 500 μm length, with pitch of 1000 μm. In order to maintain the functioning of each Si-IF output reliably, the internal contact pattern of FlexTrate™ Connector, named as Si-IF side pads hereafter, is decided to be exactly same as the fan-out pattern.

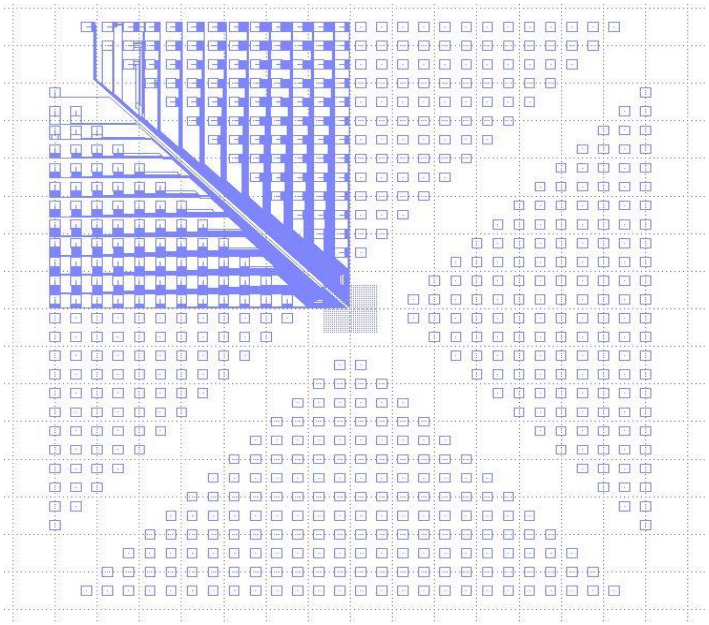


Figure 3. The schematic of the Si-IF 26 by 26 pattern.

After setting the contact of the Si-IF side pad, which is the internal system, the contacts of external system pads are needed to be determined. In the case of this work, the PCB is chosen as the external system, which is the other side of the FlexTrate™ Connector, and will be addressed as PCB side pads hereafter. In order to avoid the problems during the distributional designing, like missing pads or redundant area, the simplest method is to keep the regularity and periodicity of

the original pattern. Using this method, the first version of the PCB side pads is directly expanded from the Si-IF side pads with the same distribution but bigger pad area, as shown in Figure 4. However, there are some critical issues in the first version of PCB side pads, such as the area restriction and wire connection, and will be discussed in Chapter 2.3.

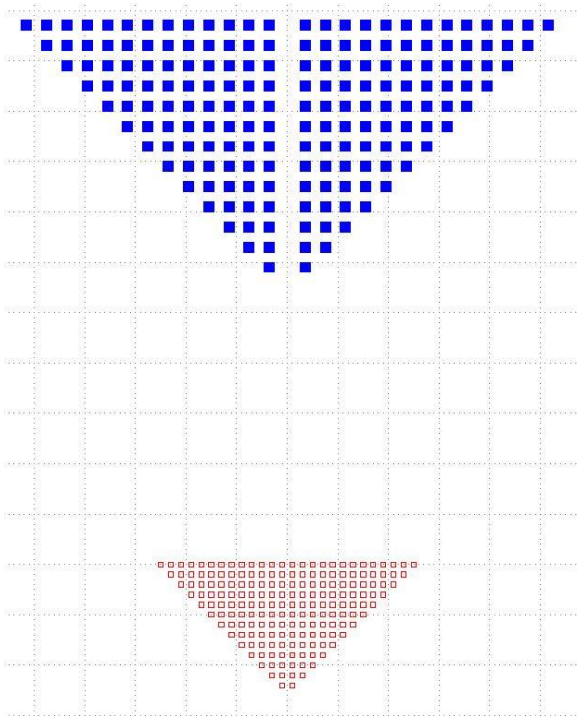


Figure 4. The design of pad distribution (internal/external) for FlexTrate™ Connector.

In the quarter of the pattern, which is 13 by 13 pads, shown in Figure 4, the red hollow part represents the Si-IF side pads while the blue solid part stands for the PCB side pads. The dimension of the PCB side pads is 1000 μm width and spacing, which equals to 2000 μm pitch in both vertical and horizontal direction. There are two reasons to fix both the width and spacing to 1000 μm. First, bigger the width of the pad, it is easier to do soldering manually, also larger the spacing between pads, more wires can be placed. Second reason is, due to the area restriction, the size of the pitch cannot be magnified infinitely. Hence, the optimized size of the pad and spacing

are decided as 1000 μm. Though the optimized size is set, there are still many problems needed to be addressed and will be discussed below.

2.3 Limitations and Solutions of Designing

In this section, several limitations and their solutions will be deliberated, such as the limitation of the PDMS area, how the wiring connects between the Si-IF side and the PCB side.

2.3.1 Area Restriction

The area of the PDMS substrate is the most critical parameter of the design. Almost all values will be influenced by the area. For example, bigger area can lead to more options of distributing the PCB pads in any customized placement. However, the reason that the bigger size of PDMS cannot be used in this work is because the process of FlexTrate^{TM} Connector (will be discussed in detail in Chapter 3) is based on a 4-inch wafer. The 4-inch wafer is the only size used in the cleanroom at UCLA, including Integrated Systems Nanofabrication Cleanroom (ISNC) at California NanoSystems Institute (CNSI) and UCLA Nanofabrication Laboratory (Nanolab). If bigger size of the wafer can be adopted, bigger PDMS substrate can be fabricated, and the limitation of the area will be reduced.

As shown in Figure 5 below, a Teflon ring (white ring area) with 5 mm width is placed at the outer peripheral area of the 4-inch wafer (orange area) for holding and protecting the gel-liked PDMS during molding. Subtracting 5mm width of Teflon ring, the remaining radius of the PDMS substrate is:

$$50\ (\text{radius of wafer}) - 5\ (\text{thickness of Teflon ring}) = 45\ \ (mm)$$

In other words, the biggest area that can be made for a FlexTrate™ Connector is a square with diagonal length equal to 90 mm. Thus, the length of the square is:

$$\frac{90\ (mm)}{\sqrt{2}} \approx 63.6\ (\text{mm})$$

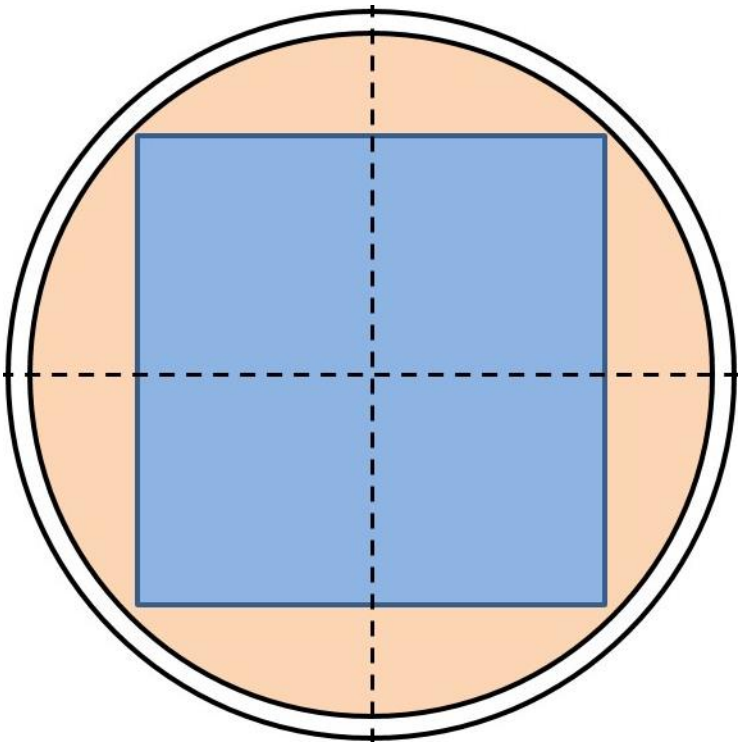


Figure 5. The area restriction of the FlexTrate™ Connector.

After knowing the area of the FlexTrate™ Connector, the distribution of the PCB side pads is as shown in Figure 6. As we can see in the Figure 6, the gray circle represents the 4-inch wafer where the Si-IF is bonded, while the green square stands for the area of PDMS. In other words, the combination of the blue/red pads, and the PDMS is the size of the FlexTrate™ Connector. Once the FlexTrate™ Connector is attached to the 4-inch wafer after aligning with the Si-IF pads, the overlap area inside the red circle is prohibited because the external pads cannot be distributed on the wafer (circled in Figure 6). Additionally, reducing the pad size is not considered as

aforementioned. Therefore, the solution of avoiding the overlap without changing the pitch is to re-distribute the pattern of the PCB side pads. After modifying, as shown in Figure 7, the final distribution is to expand the columns from 13 to 14 and move some pads to the additional column. Due to this placement, not only the overlap caused by the area limitation is solved, but also the extra spacing gave way to more possible wiring.

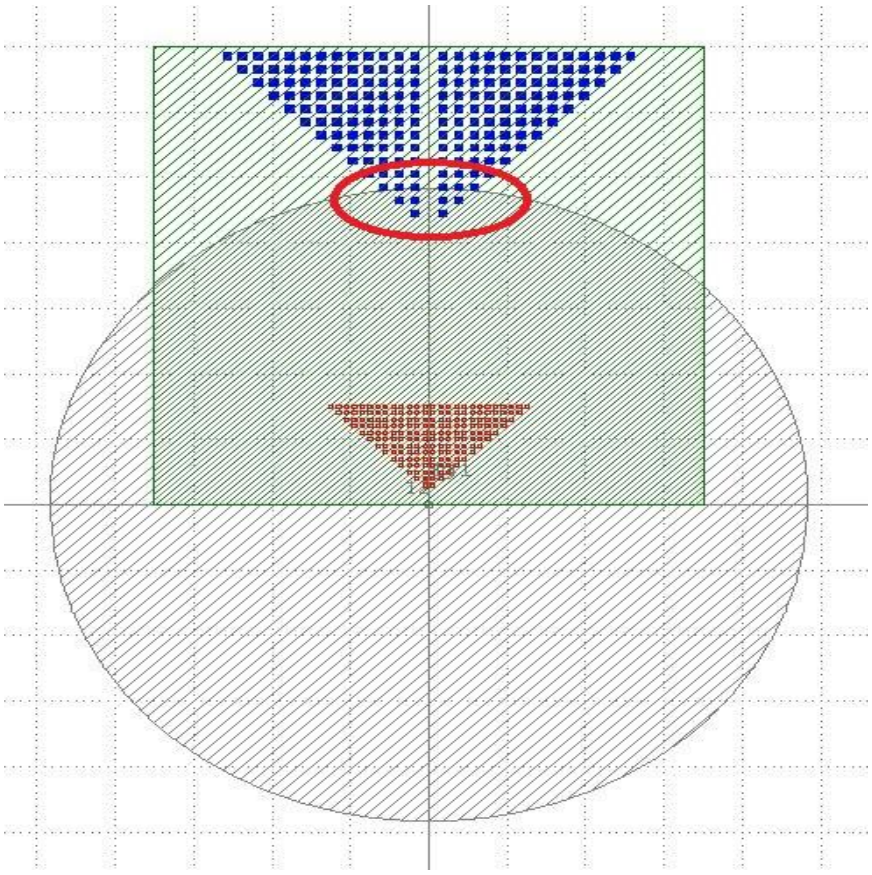


Figure 6. The sketch of the first version FlexTrate™ Connector including overlap area.

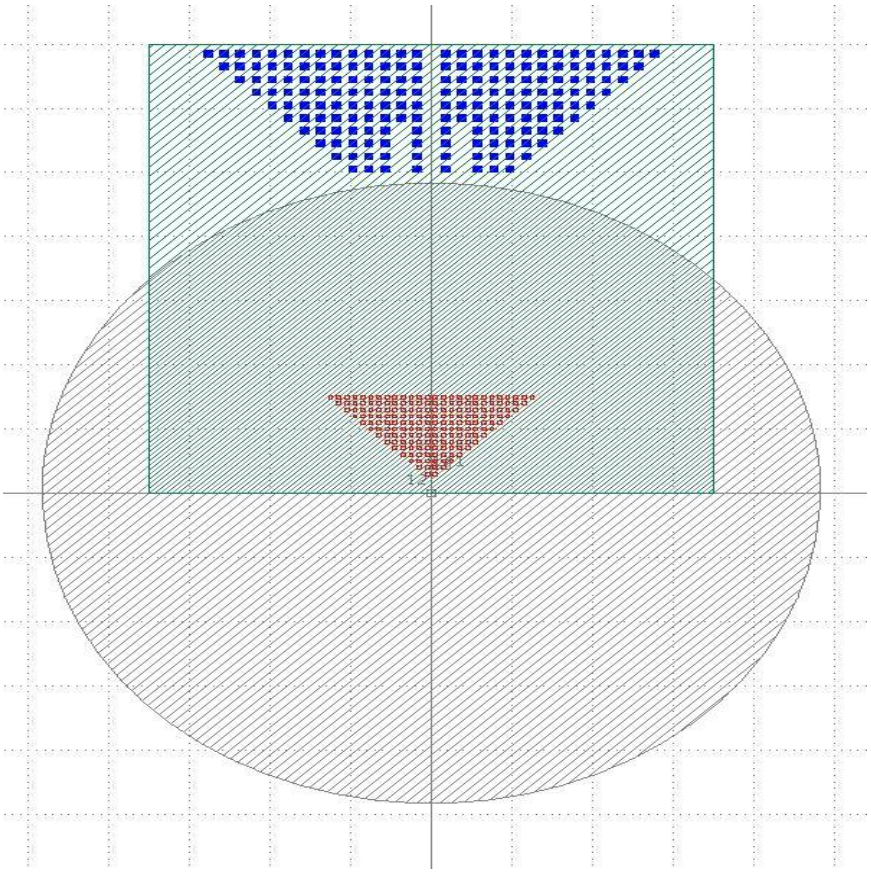


Figure 7. The final pad distribution of FlexTrate^{TM} Connector.

2.3.2 Number of the Connections

After the pattern of PCB side pads is decided, the wires need to be connected. At the very first thought, it is easy to come up with the idea that links each inner and corresponding outer pad regularly and periodically, which has already been considered when designing the pattern of the external system. As the result, the linkages of the internal and external pads connect perpendicularly (black lines) as shown in Figure 8.

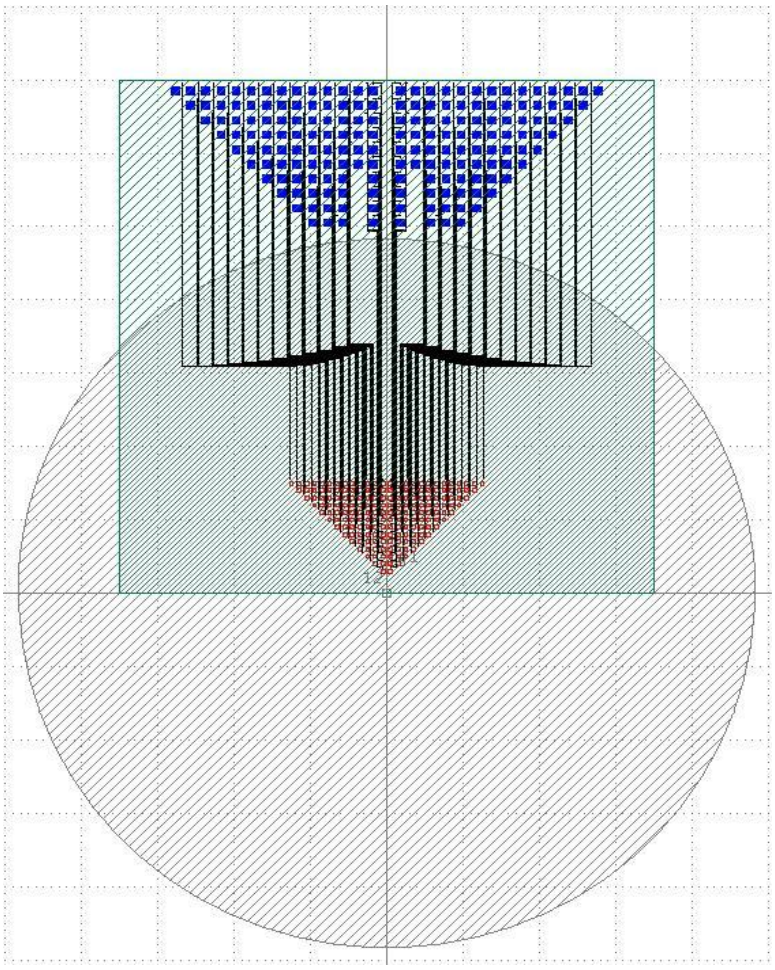


Figure 8. The designed connection for the pad of FlexTrate™ Connector.

After the wiring was done, a new consideration for the number of wires came up into this work. The FlexTrate™ Connector is designed to act as an electromechanical device that will be bent, which means there may be a probability of breakage while bending the FlexTrate™ Connector due induced stress and strain. Increasing the number of connections to a single pad is a viable solution to provide redundancy. However, the pattern of Si-IF side pads must match with the Si-IF fan-out pattern, which is already fixed. Moreover, the spacing between two pads is fixed to 500 μm. In other words, assuming the maximum number of wiring is *x*, the equation of *x* is as follow:

$$20x + 20(x-1) = 500\ (\mu m)$$

$$x = 13$$

In the equation, $20x$ represents the total width of the wires, while $20(x-1)$ stands for the total width of the spacing. As a result, the maximum number of wires is 13, while the maximum number of columns is 10, shown in Figure 7, which means there is no more space for adding the extra wires for each pad. Thus, the method of daisy chain is adopted as a solution. By using the daisy chain, the space for the wire connections is reduced to half and the extra space can be dedicated to the redundant wires for each pads as shown in the Figure 9 below. The wire for the daisy chain is designed to be much wider than the connection to avoid crack generation caused by bending.

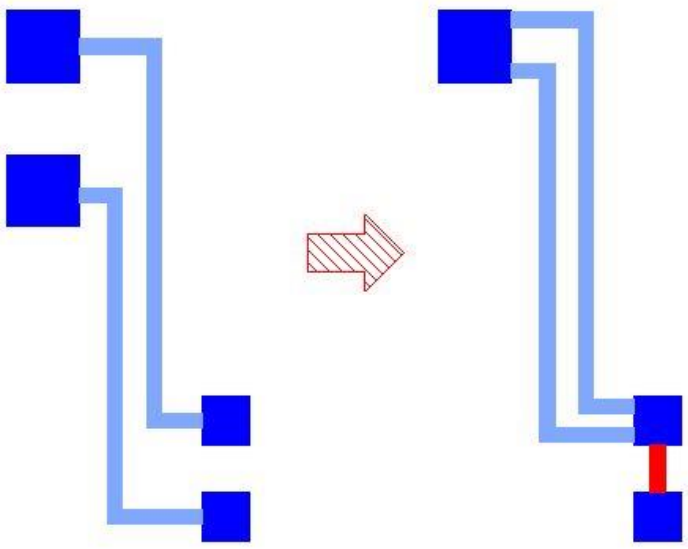


Figure 9. Schematic of daisy chain for FlexTrate™ Connector.

2.3.3 The Junction between Pads and Wire

After all the pads and connections are fixed, one last issue that needs to be solved is the junction between the pad and the wire. As discussed before, the width of the wire is 20 μm while the width of the pads are 500 μm and 1000 μm for internal and external system respectively. In this case, the dramatic change of the width from 20 μm to 500 μm or 1000 μm will lead to residual stress inside the copper wire at the junction after electroplating process and potential electromigration issue. Therefore, a triangle-shape pattern is adopted as the solution to this issue to avoid the significant variation. As shown in Figure 10, an additional triangle pattern is added to the original square pad both in the inner system and outer system, so that the residual stress at junction generated by the fabrication process of electroplating can be released in order to keep the pattern from breaking.

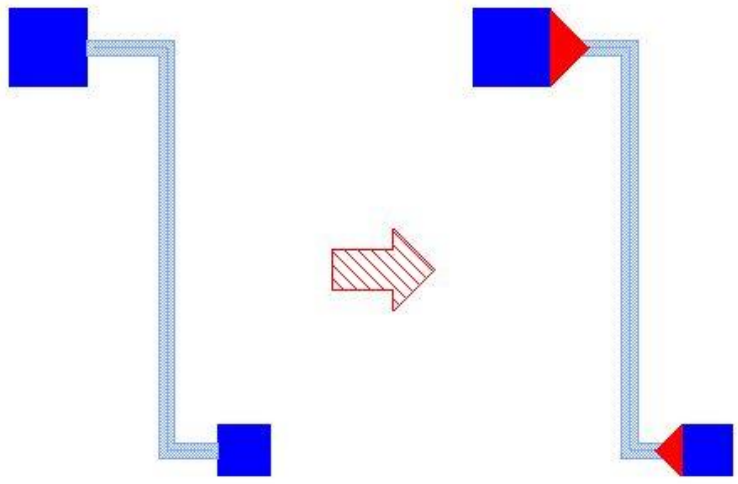


Figure 10. Schematic of junction between pads and wire for FlexTrate™ Connector.

2.4 The Final Version of the Pattern

With all the requirements discussed and determined as aforementioned, the final version of the FlexTrate^{TM} Connector is designed as shown in Figure 11 below. The gray circle stands for the 4-inch wafer while the green square is the FlexTrate^{TM} Connector, and the blue pattern represents the pads for both internal and external system and their connecting wire. By using column addition, daisy chain placement, and the triangle shape augmentation, the apparent issues of the pattern are solved. The final version is ready and the fabrication process will be introduced in the next chapter.

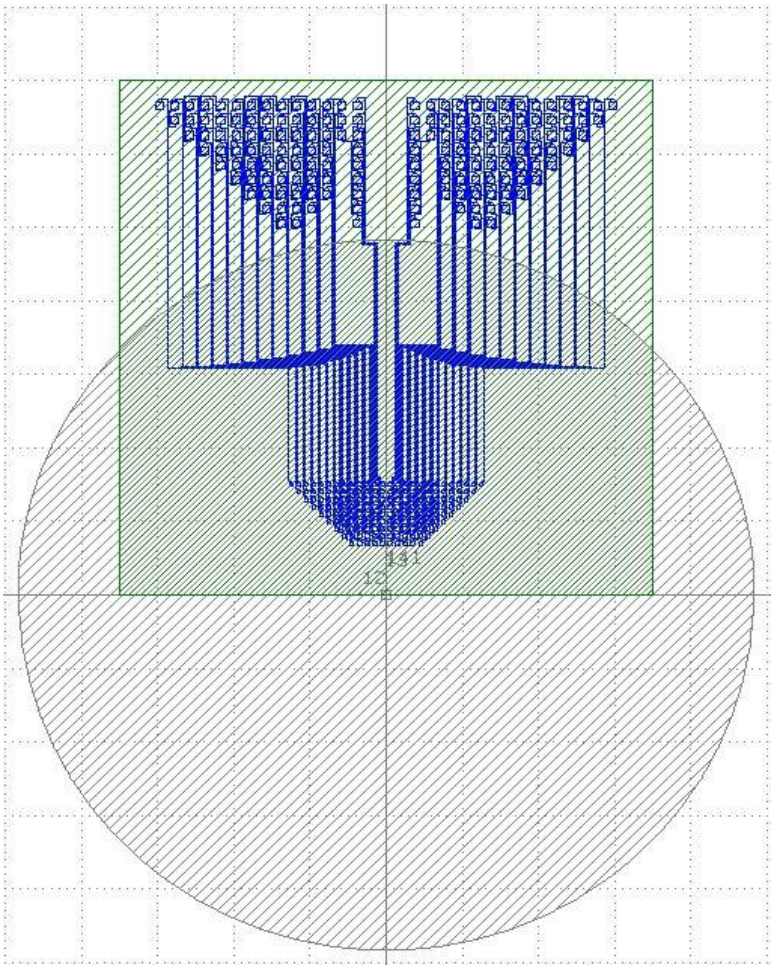


Figure 11. The final verison of the pattern for FlexTrate^{TM} Connector.

CHPATER 3

Fabrication Process of the FlexTrate™ Connector

3.1 Overview of the Fabrication Process

After the discussion of the pattern design, the fabrication of the FlexTrate™ Connector is addressed in this chapter. As mentioned above, the FlexTrate™ Connector is based on the process of FlexTrate™, which is already developed at UCLA CHIPS. The FlexTrate™ Connector process need not worry about the die shift that occurs in the general process of FlexTrate™ as there are no dies embedded in the connector. This makes the process faster and easier to achieve. All the processes introduced in the following section are carried out in the Integrated Systems Nanofabrication Cleanroom (ISNC), a class 100 cleanroom laboratory at California NanoSystems Institute (CNSI), UCLA.

3.2 Process Flow of FlexTrate™ Connector

3.2.1 First Handler and Temporary Adhesive Layer

FlexTrate™ is a flexible and bendable embedded packaging technology which uses polydimethylsiloxane (PDMS) as the substrate. The FlexTrate™ process involves molding the PDMS on a rigid substrate and curing it. A 4-inch silicon wafer is used as the supporting substrate to cure the PDMS during the transformation from a viscous liquid to a solid state. As presented in the Figure 12, a temperature-sensitive layer called thermal tape, is attached on the silicon wafer (1st handler) to act as a temporary adhesive layer. With the temporary adhesive layer, it will be

easier to release the PDMS after curing from the handler by heating to the release temperature of the tape. In this work, the release temperature of the thermal tape for 1st handler is 120^oC.

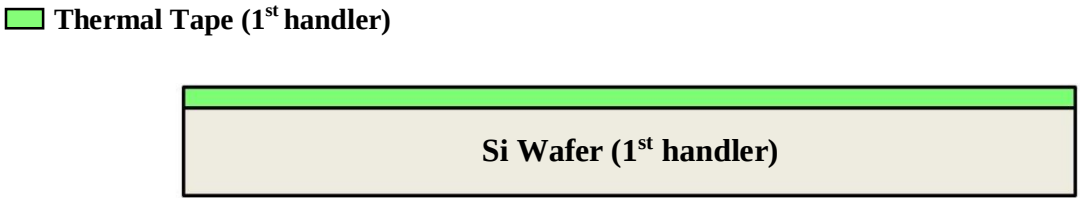


Figure 12. Schematic of first handler and temporary adhesive layer.

3.2.2 Dispensing Polydimethylsiloxane (PDMS)

After the adhesive layer is laminated on silicon wafer handler, a 5 mm wide Teflon ring is put around the periphery to contain the PDMS after dispensing.

The amount of PDMS will depend on the thickness of Teflon ring, if the PDMS is too much, it will overflow and create thickness variation from edge to center, and if the PDMS is too less, the finished-product will be porous and may have dishing issues. In the case of this thesis, 0.5 mm thickness of Teflon ring is adopted, correspondingly, 3.6g PDMS (SILASTIC MDX4-4210 Biocompatible PDMS) is added with curing agent in the ratio of 10:1, and further mixed and degassed (Thinky Mixture) with 2200 rpm for 2 minutes, then the liquid PDMS is poured into the middle of the Teflon ring.

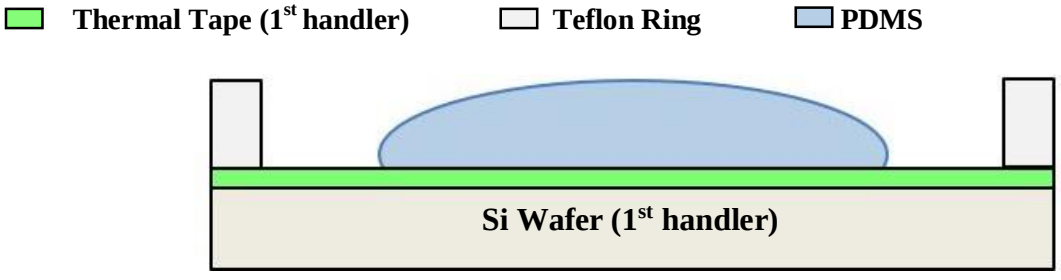


Figure 13. Schematic of the position for Teflon ring and pouring PDMS.

3.2.3 Second Handler and Molding

After the PDMS spreads, the second handler with the temperature-sensitive temporary adhesive layer is placed on it as shown in Figure 14. Since the 1st handler is removed first, the release temperature of the 1st handler (120^oC) must be lower than the 2nd handler, which in this case is 200^oC. After the 2nd handler is placed, the entire assembly consisting of the PDMS with two handlers is placed on a hot plate to cure for 30 minutes at 70^oC (or 24 hours under room temperature) [12] with a force of 5 Newton on top of the second handler to flatten the surface.

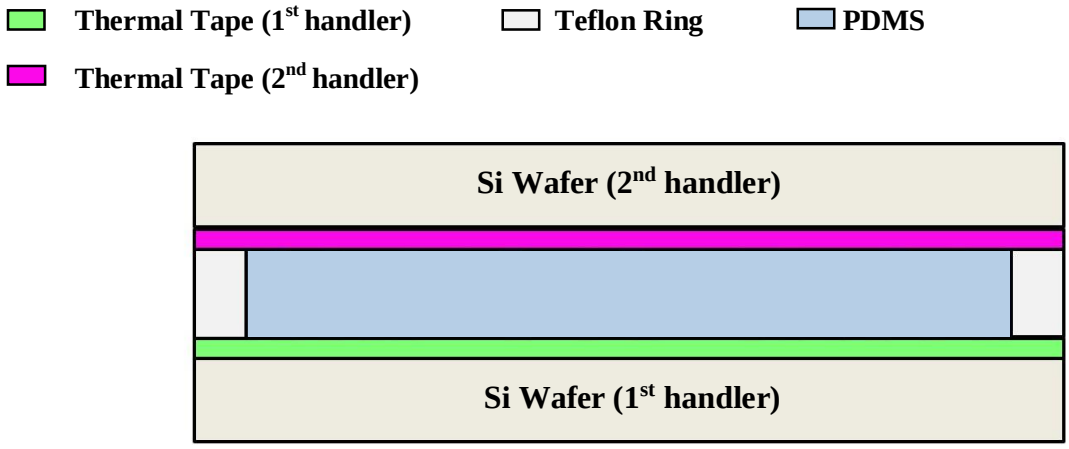


Figure 14. Schematic of the second handler and the PDMS molding.

3.2.4 Debonding (First Handler Release)

As prior introduced, after molding and curing the PDMS substrate, the 1st handler is released. The heating plate is now turned to the release temperature of the first thermal tape, which is 120^oC. The Teflon ring is also removed manually after release of the 1st handler. The PDMS is then subjected to other steps such as buffer layer and dielectric layer deposition and electroplating.

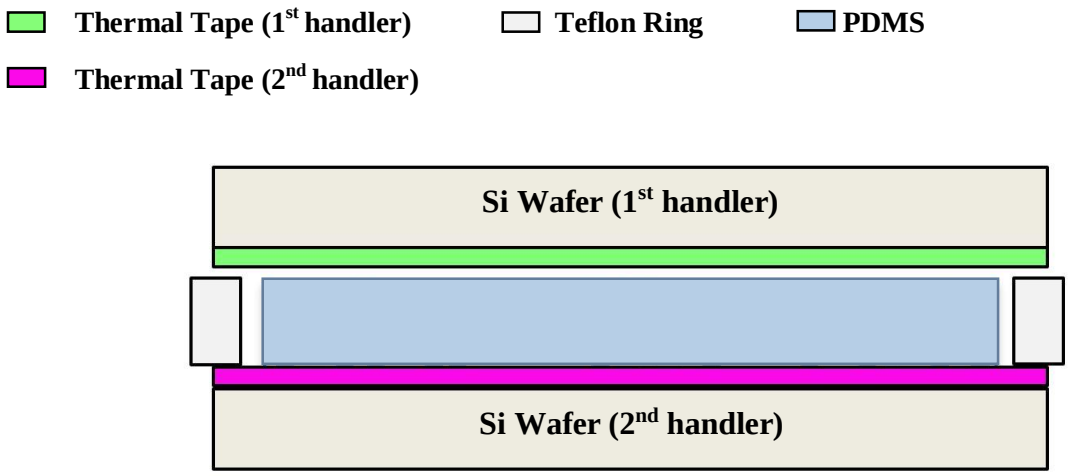


Figure 15. Schematic of first handler debonding and Teflon ring releasing.

3.2.5 Buffer Layer Deposition

After PDMS molding, the patterning and electroplating of copper are to be carried out. However, it is impossible to metalize the PDMS surface directly due to the CTE mismatch of Cu and PDMS [11]. Hence, thin stress relieving buffer layers are deposited prior to the metallization layer to release the unwanted stress [13]. A combination of two materials is chosen to act as the buffer layer, the first one, close to PDMS substrate, is parylene-C while the second is SU8-2001 [13]. Parylene-C is deposited by chemical vapor deposition (CVD) while SU8-2001 is spin coated on top of parylene-C and exposed to UV radiation (Karl Suss MA6-Contact Aligner & Lithography) to form a solid stiff layer. With this stack of layers, not only the surface of PDMS is planarized and the roughness reduced, but also the mechanical stability is increased. The criteria to choose the parylene-C and SU8-2001 are, firstly, the curing temperature must be lower than the release temperature of the 2nd handler, and secondly, the layers must be thin enough to keep the flexibility and bendability of the PDMS intact. The deposited thickness of parylene-C is 2μm via CVD (SCS

Parylene Deposition Operation 2010) for 45 minutes, while SU8-2001 is 1μm via spin-coating with 3000 rpm for 30 seconds.

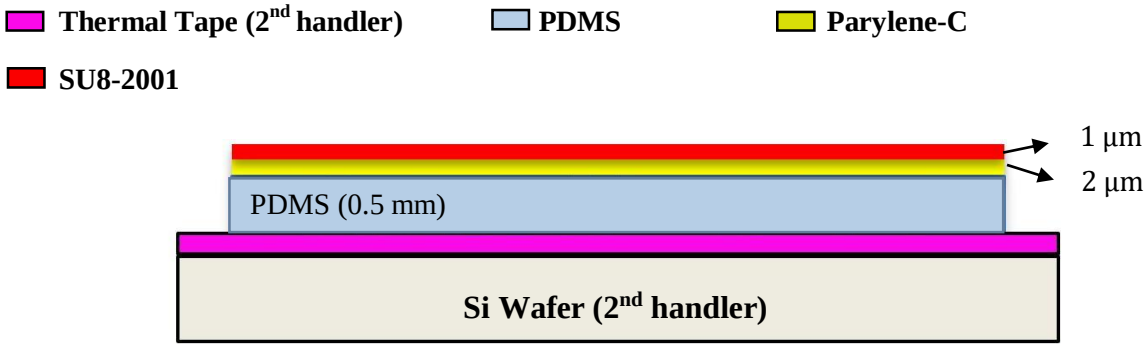


Figure 16. Schematic of buffer layer deposition.

3.2.6 Corrugation Layer Deposition

After buffer layer deposition, the next steps are patterning and metallization. However, as the FlexTrate™ Connector is an electromechanical device that should endure bending and stretching many times, the force applied to the copper wires might not be uniform, which will cause the thin copper wires to buckle or even damage easily. Accordingly, the key is to make the stress and strain on the copper wire uniform by constructing a solid teeth-liked structure, called corrugation layer [2]. The corrugation structure can redirect the force applied on the copper wires so as to protect the materials from buckling and crack generation caused by anisotropic energy.

Here, the SU8-2005 is spin-coated on the top of the SU8-2001 with 3000 rpm for 30 seconds to form a 5μm thick layer. After that, the PDMS substrate with SU8-2005 is exposed with the pattern of corrugation layer, and further rinsed with the solution of acetone, isopropyl alcohol (IPA), and DI water. The optical image of the fabricated corrugation layer is shown in Figure 17.

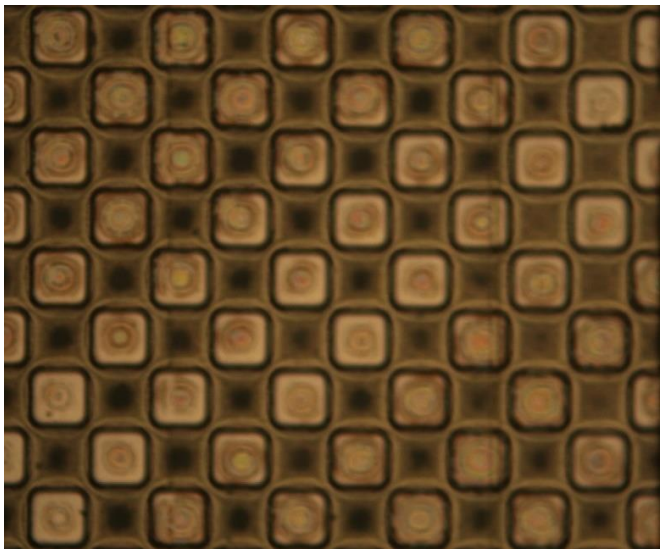


Figure 17. The corrugation layer under optical microscope.

SU8-2005 is chosen to be the material for the corrugation layer because it is the same material as SU8-2001 and hence there will not be any mechanical issue. Once the SU8 is exposed to UV radiation, the material will become stiff to support metal layer and redirect the stress along with the corrugation layer.

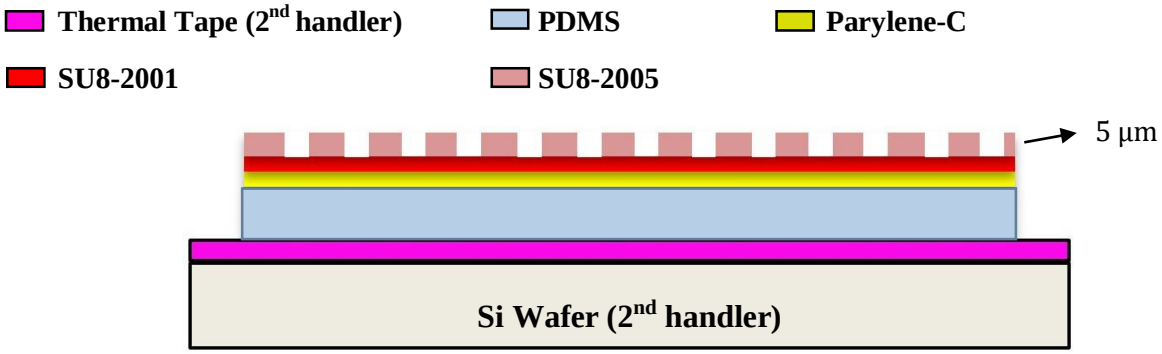


Figure 18. Schematic of corrugation layer deposition.

3.2.7 Seed Layer Deposition

Next, the metallization layer is deposited on the top. In the case of FlexTrate™ Connector, the semi-additive process is adopted to establish the metal pattern. Therefore, the metal seed layers

need to be deposited first in order to do the process of electroplating. The target materials of metal seed layers are 50 nm of titanium (Ti) and 500 nm of copper (Cu). The role of Ti here is to improve the adhesion of Cu to SU8 and as a barrier to potential Cu diffusion into the underlying layer.

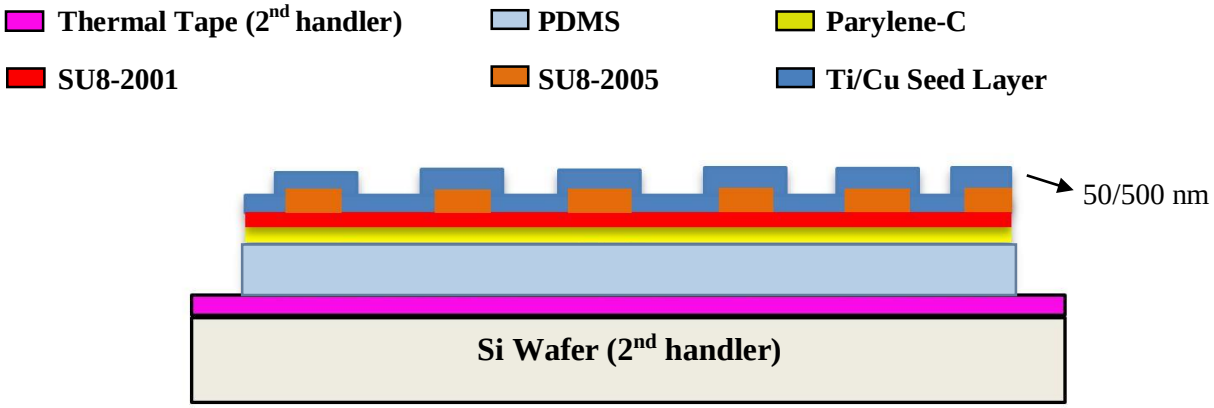


Figure 19. Schematic of seed layer deposition.

3.2.8 Imaging of Wiring Pattern

In the semi-additive process, the seed layer is deposited first, the photoresist is spin coated on the seed layer. After that, the process of imaging is carried out. However, the general substrates are flat and smooth which make the determination of the power-level and the depth of focus of the laser writing process easy. In this work, as mentioned above, there is a corrugation layer which supports the metal layer, which causes variability of the power-level and focus across the PDMS substrate. Thus, it is essential to do an experiment to determine these parameters.

In this experiment, a silicon wafer, coated with corrugation layer and photoresist, is separated into eight equal sections. Then, a testing pattern is imaged onto each of these sections by varying one parameter. The results are used to finalize the optimum power-level and the depth

of focus for the corrugation structure. After several iterations, the optimized power-level and the depth of focus have been determined for patterning. With the imaging equipment (MivaTek Laser Writer), the pattern designed is printed on the SU-8 photoresist successfully. By using the corresponding developer (MIF AZ 300), the exposed-photoresist is washed out leaving only the required pattern for further electroplating, as shown in Figure 20.

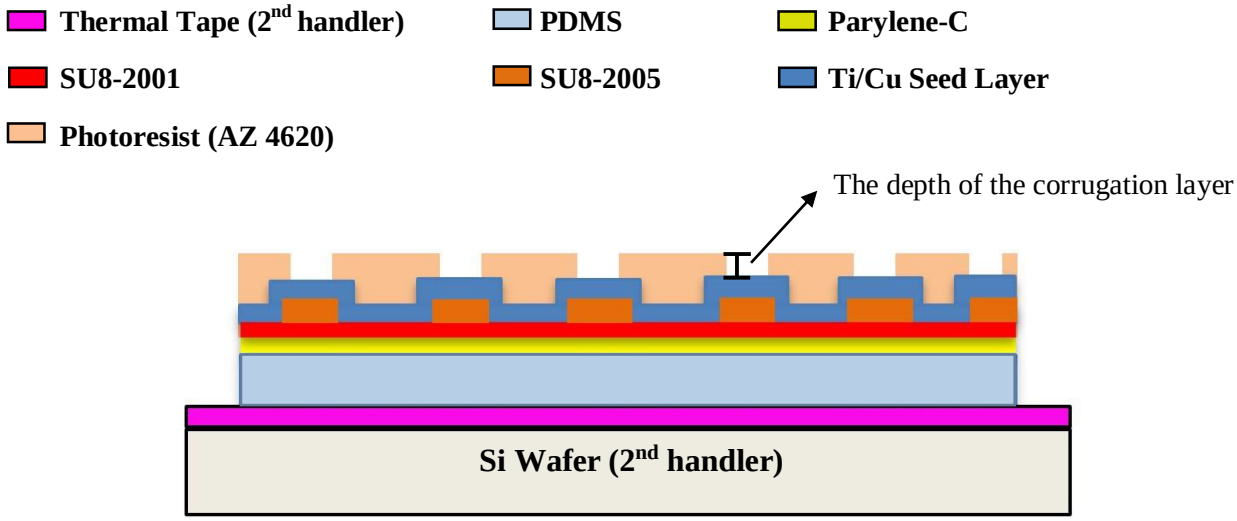


Figure 20. Schematic of wiring pattern imaging.

3.2.9 Copper Electroplating

The electroplating process is widely used in the field of packaging for metallization. In this work, the process of electroplating is adopted for Cu deposition.

The duration of electroplating is needed to proceed with the process. The following method is used to understand the plating duration for the FlexTrate™ Connector. The depth of the sample with the photoresist and the pattern opened for electroplating needs to be understood in order to calculate the plating time. However, the depth of the gap, as shown in Figure 20, is hard to estimate precisely. As mentioned above, the gap is basically generated by the corrugation layer and the coating of photoresist. The height of SU8-2005 is around 5 μm [2], while the height of the

photoresist is approximately 6μm (In this work, AZ4620 is used with the spin rate of 4000 rpm for 30 seconds) [14]. In other words, the depth range of the gap is from 5μm to 11 μm and it is not possible to determine accurately. Thus, profilometry is carried out to determine the depth (Dektak 8 Profilometer). As shown in the Figure 21, we can understand that the depth of the gap is from 5. 5 to 8μm.

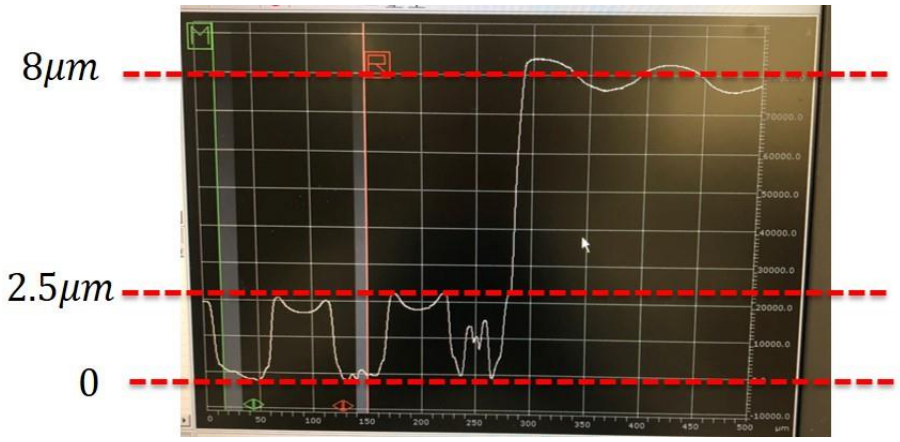


Figure 21. The depth of the gap before electroplating detected by the profilometer.

The plating rate is also needed to calculate the time. In the process of electroplating for FlexTrate^{TM}, the current is set as 60mA. During the first iteration, the sample is plated for 20 minutes. After that, profilometry is done again to detect the difference of the depth. As shown in Figure 22 below, the maximum gap is reduced from 8μm to 7μm, which means the plating rate at current of 60 mA is 50 nm/min. Finally, the complete plating of the system is carried out with the electroplating rate of 50nm/min at current of 60mA.

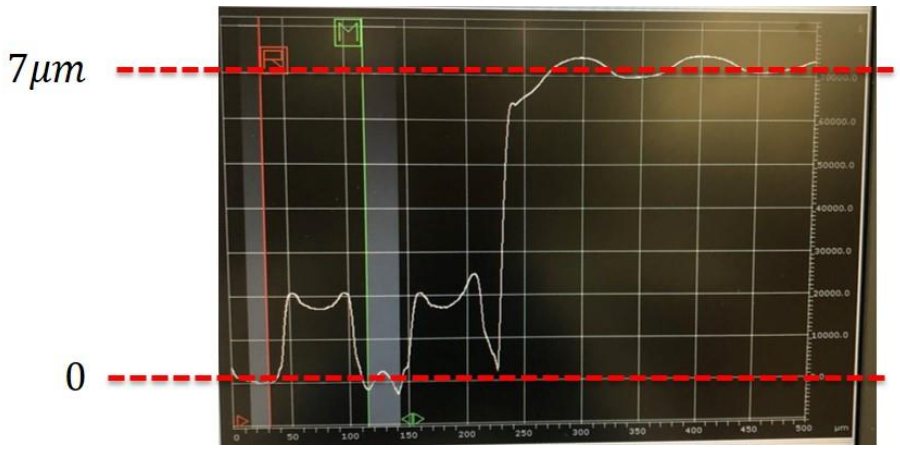


Figure 22. The depth of the gap after electroplating detected by the profilometer.

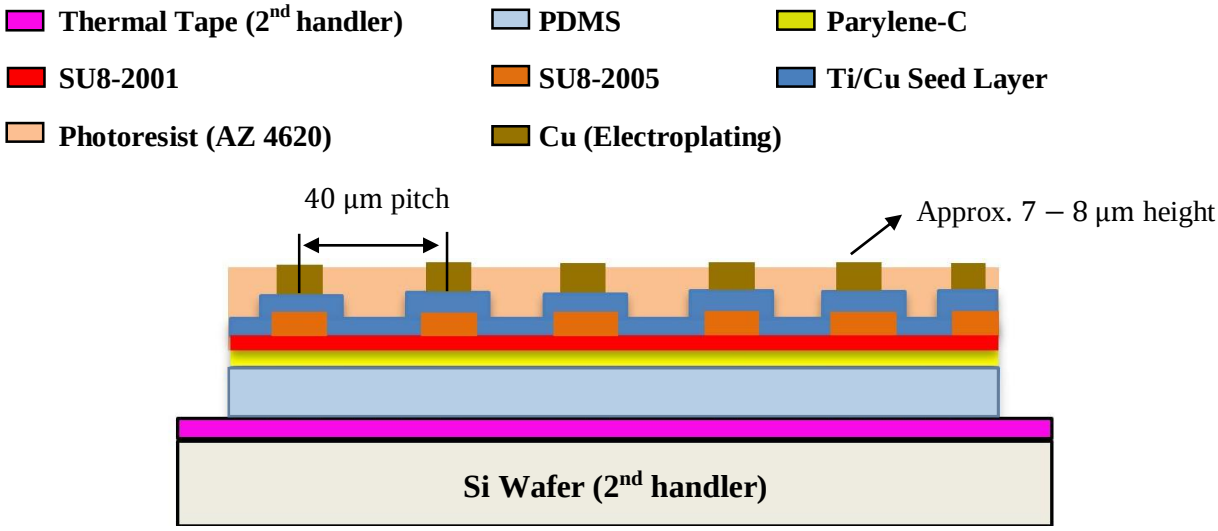


Figure 23. Schematic of electroplating.

3.2.10 Photoresist Stripping

After the electroplating is done, the photoresist is no longer needed. It is straightforward to remove the photoresist by using the solutions of acetone, IPA, and the DI water orderly. There is no need to be worried about the interaction between these solutions and the PDMS polymer because, as aforementioned, the PDMS substrate is covered by SU8-2001, which is a stable

material and acts as the protection layer for PDMS. Thus, the photoresist can be removed easily as shown in Figure 24.

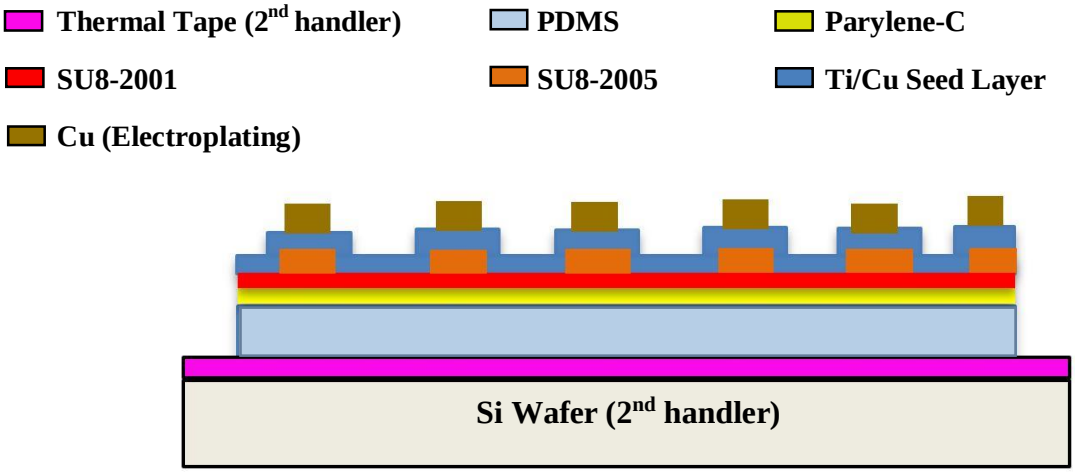


Figure 24. Schematic of photoresist stripping.

3.2.11 Etching of Metal Layers

The metal from the undesired areas is needed to be removed so as to achieve the final pattern. The methods accepted to eliminate the metal layers are introduced as follow. As mentioned above, two metal seed layers have been deposited on the top of the corrugation layer in order to electroplate, which means the etching process needs to target these two different metals, Ti and Cu respectively.

On the top of the seed layer is the 500 nm thick Cu layer, and the approach selected for cleaning Cu layer is wet etching process with the APS-100 Cu Etchant, which is provided by Transene [15, 16]. The etchant is diluted with DI water in the ratio of 1:10 so as to achieve an etching rate of approximately 40 nm/min. The APS-100 Cu etchant composes of ammonium persulfate (15-20%) and water (75-80%). The chemical reaction for APS-100 Cu Etchant is:

$$Cu + S_2O_8^{-2} \rightarrow CuSO_4 + SO_4^{-2}$$

where $CuSO_4$ is water-soluble and will be removed by the DI water in the APS-100 Cu etchant.

After that, the Ti seed layer is etched with the 6:1 buffered oxide etch (BOE) which is provided by Fisher Scientific. The etching rate is about 200 nm/min. The composition of 6:1 BOE is ammonium fluoride (34%), hydrogen fluoride (7%), and water (59%); in other words, the chemical reaction of Ti and BOE is:

$$6HF + Ti \rightarrow H_2TiF_6 + 2H_{2\,(g)}$$

where the product of the reaction, H_2TiF_6, is water-soluble and will be cleared away during the process [17].

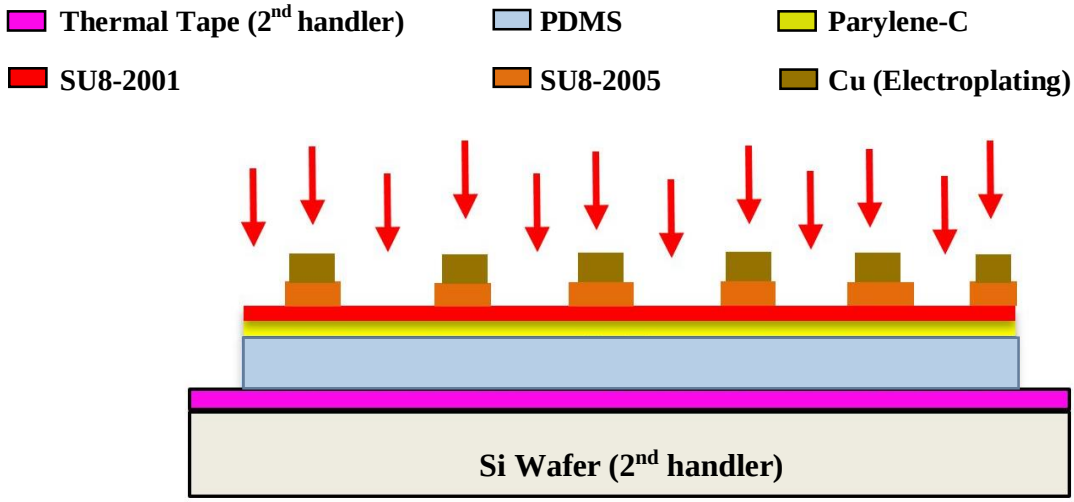
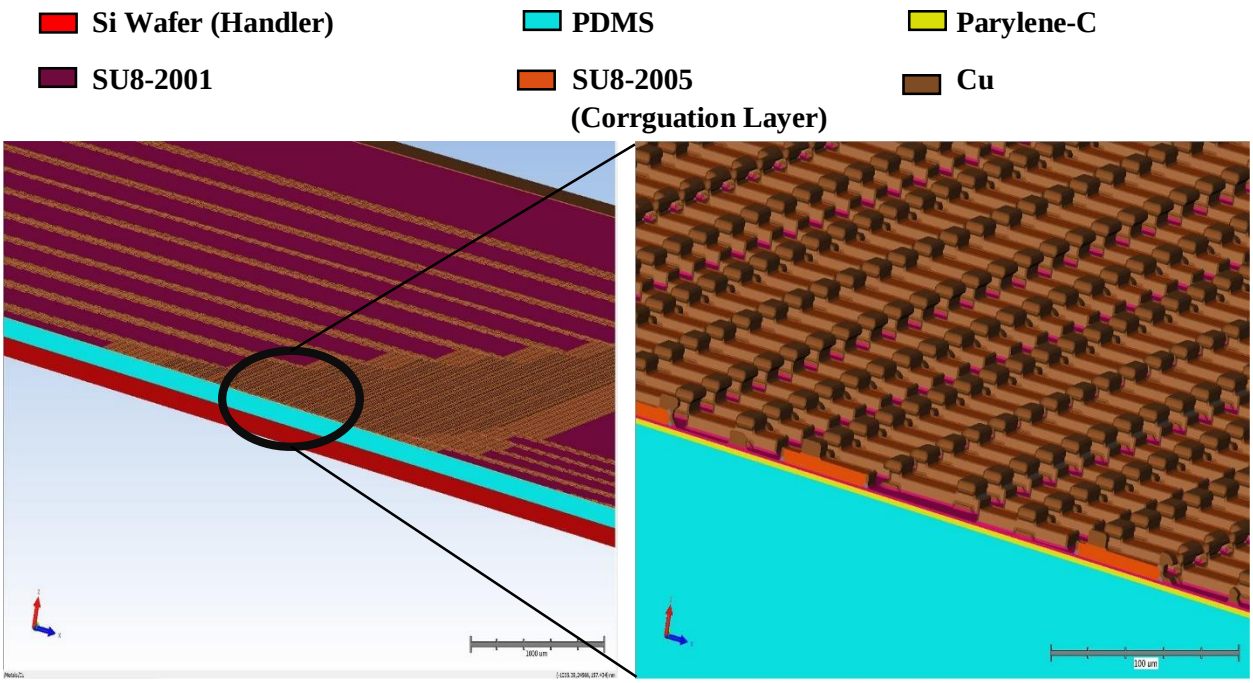


Figure 25. Schematic of metal layer etching.

A schematic of simulation, made with Coventor SEMulator3D 8, is presented in the Figure 26 to show the structures of FlexTrate™ Connector including PDMS, corrugation layer, and the Cu pattern in three-dimension model. As shown in Figure 26 (b), the corrugation layer is well construct to support the Cu pattern and prevent from the buckling and cracking.



(a) (b)

Figure 26. (a) a schematic of FlexTrate™ Connector 3D model simulation (scale: 1000μm).

(b) is the zoomed image of (a) to show the corrugation layer and the Cu wire (scale: 100μm).

3.2.12 Passivation Layer Deposition

After all the unnecessary materials are removed, the rest of the product is the desired structure. However, as shown in Figure 25, the copper pattern along with other structures are all exposed to the atmosphere if not protected. Thus, the protection layer is needed to prevent the copper pattern and other materials from contamination, corrosion, or even damage. In the previous context, it was indicated that there are many options of polymer for the passivation layer. However, the criterion for choosing the passivation polymer is that the curing temperature cannot be higher than the release temperature of the 2nd handler, which is 200^oC. Hence, parylene-C is selected again to be the passivation layer for this device because of its low deposition temperature.

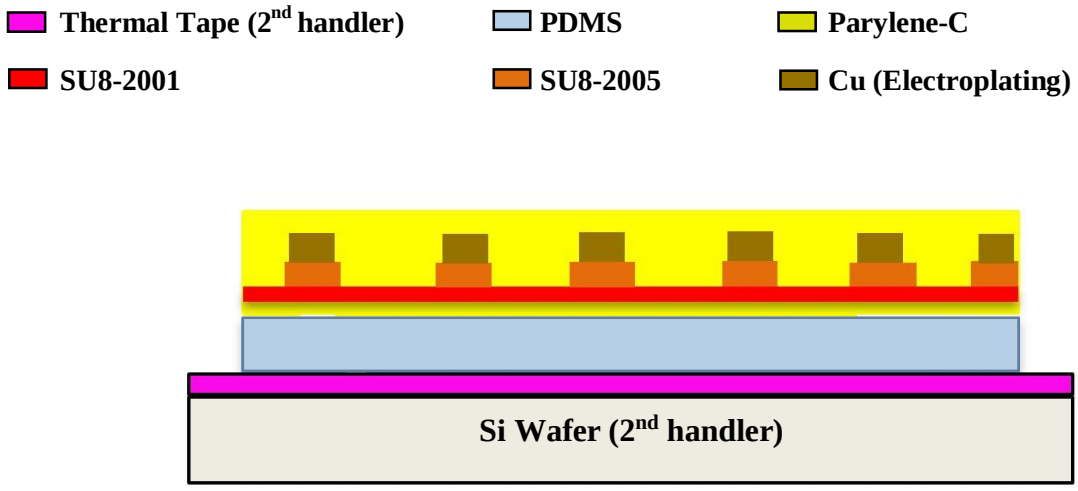


Figure 27. Schematic of passivation layer deposition.

3.2.13 Contact Imaging

In the preceding step, the passivation layer is cured to play the role of protection. However, the FlexTrate™ Connector cannot work normally without the openings for the contact since the surface is covered with the passivation layer. In order to eliminate the parylene-C on the top of the contact, the photoresist is applied on the passivation layer and exposed using the contact mask with lithography technology. After developing the exposed photoresist, reactive-ion etching (RIE) is adopted with oxygen plasma to etch the parylene-C from the open areas [18], which are the Si-IF side pads and the PCB side pads.

In order to remove the photoresist after etching, the solutions of acetone, IPA, and DI water are used.

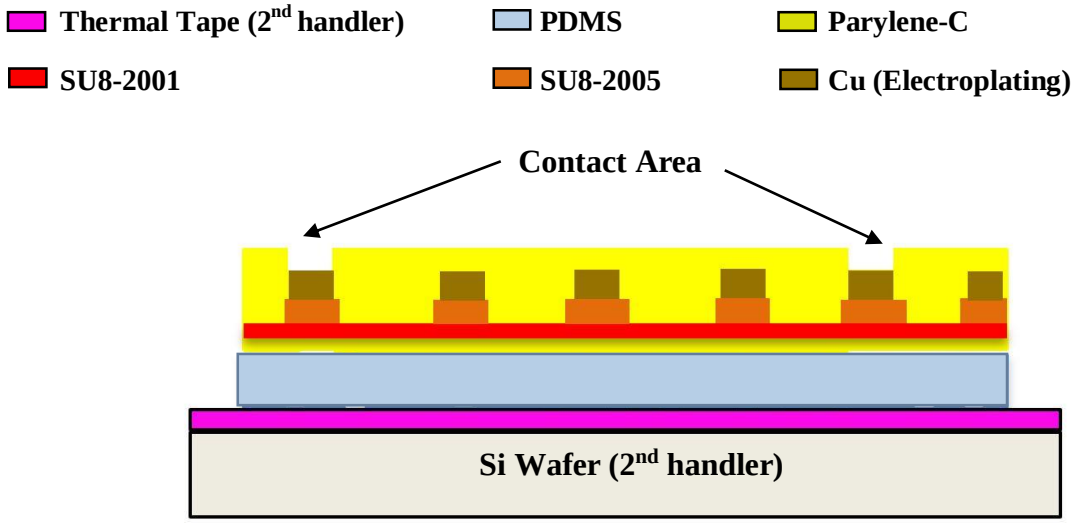


Figure 28. Schematic of contact pattern imaging.

3.2.14 De-bonding (Second Handler Release)

Since almost all the processes are completed, the last step is to release the FlexTrate™ Connector from the 4-inch silicon wafer handler. As we discussed, the PDMS substrate is adhered to a temperature-sensitive temporary adhesive layer. The temporary adhesive layer is removed from the PDMS by heating the assembly using a hot plate heated to the release temperature of the adhesive layer, in this case is $200^{o}C$.

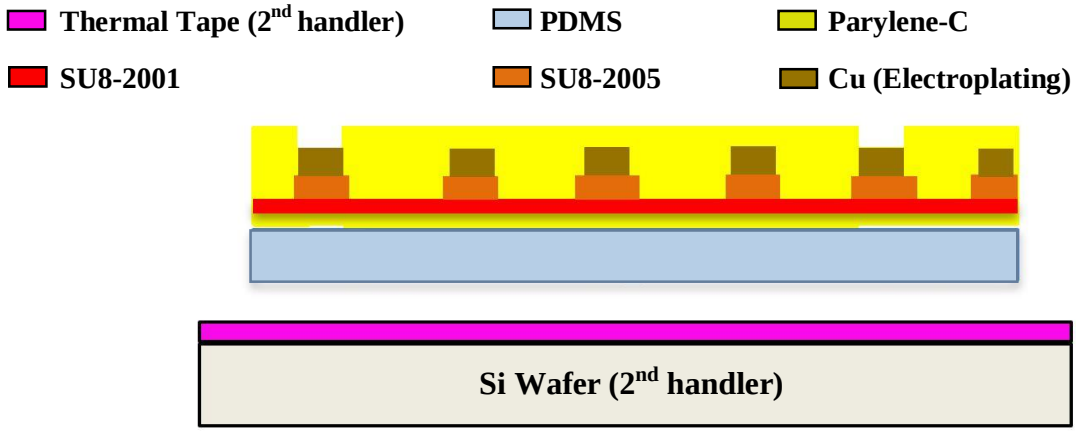


Figure 29. Schematic of second handler releasing.

FlexTrate™ Connector, a novel flexible electromechanical device, is thus fabricated with advantages of flexibility and bendability, as shown in Figure 30 With the connection of internal system, take Si-IF as an example, and external system, such as PCB, a complete circuit is accomplished which can transfer power and signal under desired frequency.

The ideal integration method is discussed in the next chapter which will include the consideration of the interaction between the FlexTrate™ Connector and the internal/external system.

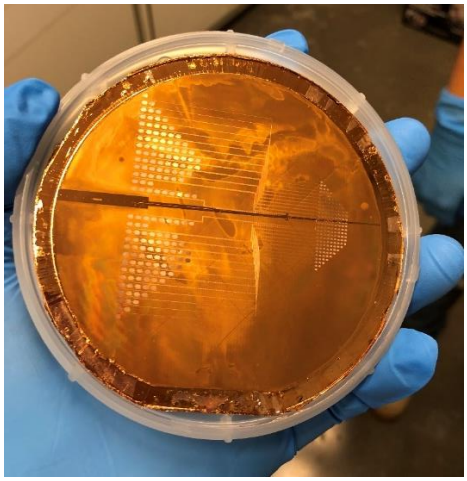


Figure 30. The FlexTrate™ Connector.

CHAPTER 4

Integration Method for the FlexTrate™ Connector

4.1 Overview of the Integration

The integration of FlexTrate™ Connector mainly deals with the method of mounting to the internal and external system. The method of integration will focus on several factors, such as the properties of the FlexTrate™ Connector and the temperature of the process. In other words, with the combination of different systems, the efficiency of the integration technology will also vary.

Here, in this chapter, the ideal method of integration is discussed, which will suit the system mentioned above, the Si-IF package is the internal system while the PCB is the external one. The integration process will primarily focus on soldering, which is one of the most mature integration technologies.

4.2 Mechanical Properties of FlexTrate™ Connector

The synthesis of FlexTrate™ Connector includes PDMS, parylene-C, SU8, and Cu. The excellent ductility and malleability of Cu, with relatively high Young's Modulus of 130 GPa [19], makes it resistant to crack or fatigue during integration. The crosslinking inside the structure of PDMS makes it a thermosetting polymer after the curing process. This makes PDMS easy to retain its shape and bonding with strong covalent bonds under high-temperature until decomposition [20].

Thus, the rest of the layers, which are parylene-C and SU8, will be the materials considered in the process of integration.

In literature, the cracking of parylene-C is observed during the reflow process of soldering, especially when heating up to 250^oC or higher [21, 22]. Some hypotheses have been proposed to explain the cracking of parylene-C. The different rates of the thermal expansion and the shrinking during heating and cooling of parylene-C causes the thermal stress and further initiates cracking [21].

Also, the properties of SU8 indicate that although it is relatively stable after cross-linking, the shrinkage will still occur when the temperature reaches to 270^oC [23]. The mechanical interaction between SU8 and parylene-C will lead to issues, such as residual thermal stress. This kind of mechanical problems will contribute to the deformation of the structure, and result in cracking [24, 25]. Thus, high temperature soldering cannot be used for the integration of FlexTrate^{TM} Connector.

4.3 Low-Temperature Soldering

According to the American Welding Society (AWS), welding can be separated into brazing and soldering; process using temperature higher than 450^oC is called brazing while lower than 450^oC is called soldering. Soldering technology is one of the popular methods for the electrical device with high-volume assembly. However, some soldering processes comprise of the reflow step, which is a process that helps the electrical components attach to the contacts. Sometimes the peak temperature of the reflow process will be higher than the melting point of the solder.

As an example, SAC305 is adopted in the integration process of the prototype of the FR-4 based periphery connector. SMD4300SNL250T3 is chosen as the solder paste which includes the Pb-free water-soluble SAC 305 product [26]. According to the datasheet, the alloy consists of Sn (96.5%), Ag (3%), and Cu (0.5%), which provide a good soldering performance. The melting point is around 220^oC and it will not influence the parylene-C and SU8 polymer layers . However, as shown in Figure 31 , the ideal profile of the reflow process for SAC305 recommended by the solder paste manufacturer indicates that the highest temperature in the reflow process will reach up to 249^oC, which might cause the thermal stress between the surface of parylene-C and SU8 and further generate the crack or even damage the Cu wire. Thus, in the case of FlexTrate^{TM} Connector, in order to avoid the mechanical issues mentioned above, the low-temperature soldering is used to suit this integration process.

There are many commercial options for low-temperature soldering alloy with reliable and precise datasheet. Many of them are made of Pb as its alloy has a relatively low melting point (less than 200^oC). However, with the core value of environmentally friendly materials, the solder consisting of Pb is not considered in this work. Here, two low-temperature solders are recommended for soldering of FlexTrate^{TM} Connector. One is InSn 118 (Indium Corp. Indalloy® 1E In-Sn Solder Alloy) [27], another one is InBi 162 (Indium Corp. Indalloy® 162 In-Bi Fusible Alloy) [28]. The properties are shown in Table 1. The melting points of these two solder alloy are both lower than 200^oC, which can be considered as a good solder for FlexTrate^{TM} Connector that will not generate the thermal stress to damage the Cu wire in the process of integration.

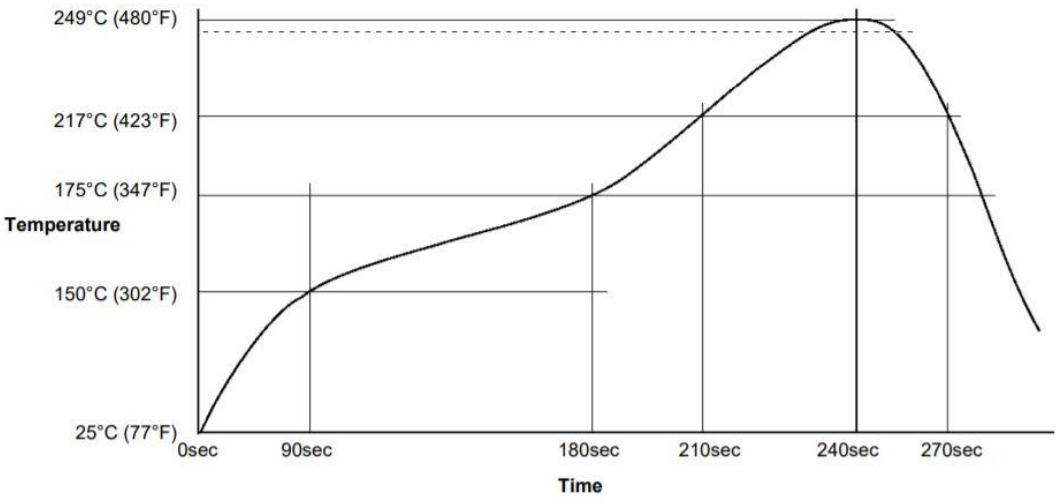


Figure 31. The ideal reflow profile for SAC 305 solder paste. [26]

Table 1. The properties of InSn118 and InBi162 from the datasheet of manufacturer. [27, 28]

Solder Alloy	**Density**	**Melting Point**	**Percentage of In**	**Percentage of Rest**
InSn 118	7.3 (g/cc)	$118.0^{o}C$	52.0% of Indium (In)	48% of Tin (Sn)
InBi 162	7.99 (g/cc)	$72.0^{o}C$	66.3% of Indium (In)	33.7% of Bismuth (Bi)

CHAPTER 5

Conclusion and Future Work

5.1 Conclusion

In the content of this thesis, several topics have been discussed: (1) the concept the FlexTrate™ Connector, which adopts the technology of FlexTrate™ and further applies on the Silicon Interconnect Fabric; (2) the pattern designed on the FlexTrate™ Connector and how the challenges are solved; (3) the fabrication process of FlexTrate™ Connector; (4) the criteria of integration method for FlexTrate™ Connector.

Comparing with the prototype of the FR-4 based periphery connector, FlexTrate™ Connector reduces mechanical issues and can fit many shapes and structures due to its better elongation, flexibility, and bendability.

In the context of the design, various challenges have been addressed, and the solutions have been demonstrated. For the fabrication, the process of FlexTrate™ Connector is optimized profitably to reduce the processing time and develop the parameters of the imaging system in order to match with FlexTrate™ Connector. The criteria of integration have been discussed, and additionally, some possible solders have been recommended to be considered for connecting the FlexTrate™ Connector to Si-IF and PCB. Finally, a FlexTrate™ Connector is made after deliberately considering all the factors.

5.2 Future Work

In future work, several characterizations and testing can be done to analyze the performance of FlexTrate^{TM} Connector. In the area of electrical characterization, the connectivity of the solder and the resistance of wires can be tested by the multimeter. Instead of examining one by one, the testing can be efficient through the daisy chain connection in both FlexTrate^{TM} Connector and Si-IF package. Moreover, the dielectric loss and the maximum frequency can be measured so that the pattern of design can be modified to match the requirement.

In the field of mechanical characterization, the shearing and thermal-cycling test can be done to understand the behavior of FlexTrate^{TM} Connector with different applied force. Furthermore, the flexibility and bendability can be investigated to learn the relation between bending and the damage of Cu wire. Last but not least, the reliability of the process can be assessed in order to maintain the effectiveness of FlexTrate^{TM} Connector.

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[27] MatWeb Material Property DATA, "Indium Corp. Indalloy® 1E In-Sn Solder Alloy"

[28] MatWeb Material Property DATA, "Indium Corp. Indalloy® 162 In-Bi Fusible Alloy"